IN THE CLAIMS

Please amended claims 25, 27, as follows below.

Please add new claim 52 as follows below.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

Marked Up Listing of Claims:

1-24. (Cancelled)

25. (Currently Amended) A memory in an integrated circuit to conserve power comprising:

a plurality of memory clusters, each of the plurality of memory clusters including

one or more memory blocks to store data, and

an output multiplexer coupled to the one or more memory blocks, the output multiplexer to output data from one of the one or more memory blocks out of the memory cluster;

a memory controller to receive addresses to the memory and control the flow of data into and out of the memory; and

a plurality of buses and control lines coupled between the plurality of memory clusters and the memory controller to propagate address and data there-between and to control the activity of the plurality of memory clusters.

26. (Original) The memory of claim 25, wherein

one of the control lines between the memory controller and the plurality of memory clusters is active to activate one of

the plurality of memory clusters while others are inactive to conserve power.

27. (Currently Amended) The memory of claim 25, wherein

each output multiplexer of each memory cluster couples to one of the plurality of buses between the plurality of memory clusters [[,]] and the memory controller ~~to output data from one of the one or more memory blocks out of the memory~~, and

each output multiplexer includes

a bus multiplexer having inputs and an output, the inputs of the bus multiplexer coupled to the one or more memory blocks of the memory cluster to receive data, and

a bus state keeper coupled to the output of the bus multiplexer and the one of the plurality of buses between the plurality of memory clusters and the memory controller.

28. (Original) The memory of claim 27, wherein

one of the control lines between the memory controller and the one of the plurality of memory clusters is inactive to conserve power and

the bus state keeper maintains the state of the one of the plurality of buses between the plurality of memory clusters and the memory controller.

29. (Original) The memory of claim 25, wherein

the memory controller includes

a plurality of bus state keepers coupled to some of the plurality of buses between the plurality of memory clusters and the memory controller.

30. (Original) The memory of claim 29, wherein

one of the control lines between the memory controller and the one of the plurality of memory clusters is inactive to conserve power and

the plurality of bus state keepers coupled to some of the plurality of buses between the plurality of memory clusters and the memory controller maintain the state of the some of the plurality of buses.

31. (Original) The memory of claim 25, wherein

one of the memory clusters is activated by one of the control lines while other memory clusters are deactivated by the other ones of the control lines to conserve power.

32-39. (Cancelled)

40. (Previously Presented) A memory in an integrated circuit to conserve power, the memory comprising:

a memory array organized into one or more memory clusters, each of the one or more memory clusters including

a plurality of memory blocks to store data, each of the plurality of memory blocks including

a plurality of memory cells,

row and column address decoders to access selected memory cells,

sense amplifiers to determine the data stored in the selected memory cells accessed by the row and column address decoders, and

tri-state drivers to store data into the selected memory cells accessed by the row and column address decoders,

and,

data bus interface logic coupled to the plurality of memory blocks, a cluster data input bus, and a cluster data output bus, the data bus interface logic to multiplex data from the cluster data input bus into the plurality of memory blocks and to multiplex data from the plurality of memory blocks onto the cluster data output bus;

and,

a memory controller coupled to the memory array, a memory data input bus, and a memory data output bus, the memory controller to receive addresses for selected memory cells of the memory array, to control the flow of input data from the memory input bus into one or more cluster data input buses, to control the flow of output data from one or more cluster data output buses onto the memory data output bus, and to control the activity of the one or more memory clusters to conserve power.

41. (Previously Presented) The memory of claim 40, wherein,

the data bus interface logic includes

an output multiplexer coupled to the plurality of memory blocks, in response to an address the output multiplexer to select one of the plurality of memory blocks to output data from selected memory cells therein and drive it onto a data output bus, and

an input multiplexer coupled to the plurality of memory blocks, in response to an address the input

multiplexer to select one of the plurality of memory blocks to receive data from a data input bus and store it in selected memory cells of the selected memory block;.

42. (Previously Presented) The memory of claim 40, wherein,

the bus interface logic includes

one or more tristate output bus drivers respectively coupled to one or more block data output buses of the one or more memory blocks to receive data out, each of the one or more tristate output bus drivers coupled to the cluster data output bus to selectively drive data out of the memory cluster onto the cluster data output bus,

one or more tristate input bus receivers respectively coupled to the cluster data input bus to receive data in, each of the one or more tristate input bus receivers respectively coupled to one or more block data input buses of the one or more memory blocks to drive data into the memory cluster,

a data bus interface controller coupled to the enable inputs of the one or more tristate output bus drivers and the one or more tristate input bus receivers, the data bus interface controller to control the one or more tristate output bus drivers and the one or more tristate input bus receivers to multiplex input data into the memory cluster and output data out of the memory cluster.

43. (Previously Presented) The memory of claim 40, wherein

the memory controller includes

a plurality of bus state keepers coupled to buses between the one or more memory clusters and the memory controller.

44. (Previously Presented) The memory of claim 43, wherein

at least one of the control lines between the memory controller and the one of the plurality of memory clusters is inactive to conserve power and

at least one of the plurality of bus state keepers to maintain a state of at least one bus between the one or more memory clusters and the memory controller.

45. (Previously Presented) The memory of claim 40, wherein

one of the one or more memory clusters is activated by one of a plurality of control lines from the memory controller, and

other ones of the one or more memory clusters are deactivated by other ones of the plurality of control lines from the memory controller to conserve power.

46. (Previously Presented) A memory in an integrated circuit to conserve power, the memory comprising:

a memory array organized into one or more memory clusters;

a memory controller coupled to the memory array, a memory data input bus, and a memory data output bus, the memory controller to receive addresses for selected memory cells of the memory array, to control the flow of input data from the memory input bus into the one or more memory clusters, to control the flow of output data from the one or more memory clusters, and to

control the activity of the one or more memory clusters to conserve power;

a plurality of data input buses coupled between the memory controller and the memory array; and

wherein the memory controller includes a plurality of bus state keepers coupled to the plurality of data input buses.

47. (Previously Presented) The memory of claim 46, further comprising:

a plurality of control lines coupled between the memory controller and the memory array; and

wherein one of the one or more memory clusters is activated by one of the plurality of control lines, and other ones of the one or more memory clusters are deactivated by other ones of the plurality of control lines to conserve power.

48. (Previously Presented) The memory of claim 46, further comprising:

a plurality of control lines coupled between the memory controller and the memory array; and

wherein at least one of the control lines to inactivate at least one of the memory clusters to conserve power and at least one of the plurality of bus state keepers to maintain a state of at least one bus of the plurality of data input buses.

49. (Previously Presented) The memory of claim 46, further comprising:

one or more address input buses coupled between the memory controller and the memory array; and

wherein the memory controller further includes one or more

bus state keepers respectively coupled to the one or more address input buses.

50. (Previously Presented) The memory of claim 49, wherein

the one or more bus state keepers to maintain a state of at least one of the one or more address input buses to conserve power.

51. (Previously Presented) The memory of claim 46, wherein

the plurality of bus state keepers to maintain a state of at least one of the plurality of data input buses to conserve power.

52. (New) The memory of claim 25, wherein

each output multiplexer of each memory cluster couples to one of the plurality of buses between the plurality of memory clusters and the memory controller, and

each output multiplexer includes a plurality of tristate bus drivers.